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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/767,046 | 01/29/2004 | Todd Michael Burdine | ROC920030281US1 | 4807 |

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| EXAMINER | |
|---|---|
| CHUNG, PHUNG M | |
| **ART UNIT** | **PAPER NUMBER** |
| 2138 | |

DATE MAILED: 03/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/767,046 | BURDINE, TODD MICHAEL | |
| | Examiner | Art Unit | |
| | Phung My Chung | 2138 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

***Claim Rejections - 35 USC § 112***

1. Claims 1-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 1, 8 and 15, lines 1-2, the preamble of these claims are " method of identifying one or more defective shift register latches in a scan chain", but there isn't any step for identifying one or more defective shift register latches in a scan chain in the body of these claims. Appropriate correction is required.

As per claims 2-7, 9-14 and 16-20 are also rejected because they dependent upon the rejected base claims.

***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3, 7-10, 14-17 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant admitted prior art (AAPA).

As per claim 1, the AAPA discloses first and second methosd, comprising:

electrically coupling a plurality of shift register latches (210) into a series configuration so as to form a scan chain circuit, wherein each of the shift register latches includes a first latch and a second latch connected in a master-slave latches includes a first latch (310) and a second latch (318) connected in a master-slave configuration, wherein each of the first latch and second latch includes at least one clock input (paragragph (0006)- (0007) and Fig. 3);

the first method, comprising: placing the scan chain circuit into an operating region, and

loading a scan test pattern into the scan chain circuit ( lines 4-5 of paragraph (0012)) ;

placing the scan chain circuit into a failing region (lines 8-9 or paragraph (0012);

applying a shift clock pulse to the clock input of the second latch (lines 9-10 of paragraph (0007)); and

the second method, comprising:

placing the scan chain circuit into an operating region, and

unloading the scan chain (paragraph (0013). The AAPA does not disclose the combination of these two method. However, the AAPA, lines 4-6 of paragraph (0016) discloses that a third defect or inner defect can be detected by either separately or combined of these methods. Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to combine the first and second methods into one method steps so that multiple defects can be detected.

As per claim 3, the AAPA further discloses loading a scan test pattern into the scan chain circuit includes loading a scan test pattern to all zeroes (lines 5-6 or paragraph (0012)).

As per claim 7, the AAPA further discloses applying a scan clock pulse to the clock input of the first latch and a shift clock pulse to the input of the second latch (0007);

measuring an output of the second latch against an expected response (RML);

recording the result; and

repeating the applying, the measuring and the recording steps until the scan chain is completed. (0012).

As per claim 8, 15 and 21-22, these claims are rejected under similar rationale as set forth in claim 1.

As per claims 9 and 16, these claims are rejected under similar rationale as set forth in claim 2.

As per claims 10 and 17, these claims are rejected under similar rationale as set forth in claim 3.

As per claim 14, this claim is rejected under similar rationale as set forth in claim 7.

4. Claims 2, 4-6, 11-13 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant admitted prior art (AAPA) as applied to claim 1 above, and further in view of Guo et al ("A Technique for Fault Diagnosis of Defects in Scan Chains", IEEE, 2001,ITC international test conference, pager 10.2, pgs. 268-277).

As per claim 2, the teaching of the AAPA has been discussed above. The AAPA does not specifically disclose analyzing the scan chain result after the unloading. However, Guo does disclose an analyzing circuit for analyzing the scan chain result (pg. 268, col. 1, section 1,

lines 1-6). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the analyzing circuit for analyzing the scan chain result as taught by Guo into the invention of the AAPA to analyze the scan chain result to isolate the cause of failure to enable design or fabrication proces mofification to avoid similar failures.

As per claims 4-6, the teaching of the AAPA has been discussed above. The AAPA does not disclose loading the scan test pattern into the scan chain circuit includes loading all ones or loading zero and ones. However, Guo discloses loading the scan test pattern into the scan chain circuit includes loading all ones or loading zero and ones (pg. 271, section 4.1). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to load the scan test pattern into the scan chain circuit includes loading all ones or zero and ones as taught by Guo into the scan chain circuit of the AAPA to detect stuck-at faults.

As per claims 11-13 and 18-20, these claims are rejected under similar rationale as set forth in claims 4-6.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phung My Chung whose telephone number is 571-272-3818. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571- 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Phung My Chung
Primary Patent Examiner